AMENDMENTS

In the Specification

Please substitute the following clean copy paragraph/page text for the pending paragraph/page text of the same number.

For the paragraph beginning on page 7, line 1, please substitute the following paragraph:

Illustrated in Fig. 3A is a block diagram of a possible example of a carry save adder 100 redesigned for performing addition on a newly encoded Propagate-Kill-Generate (PKG) input and a traditional binary bit. A PKG input is provided by a PKG recoding operation that involves recoding logic values. As mentioned before, illustrated in FIG. 1 is a recoding table 2 illustrating the encoding of two logical values into mousetrap logic. The mousetrap logic values are then encoded into PKG recoding values to reduce the number of wires routed over an integrated circuit from four wires to three wires. As can be seen in FIG. 3A, the P 101, K 102 and G 103 signals are received by the modified carry save adder 100. The P 101, K 102 and G 103 signals are input along with carry-in signal CI 104, representing one traditional binary bit carry-in number.

In the Claims

Please substitute the following clean copy text for the pending claims of the same number.

1. (Once Amended) An apparatus performing the addition of a PKG recoded number, said apparatus comprising:

a circuitry configured to receive at least a first value and a second value, wherein said second value is at least one of a P value, a K value, and a G value of a PKG recoded number; and

wherein said circuitry generates a sum value and a carry value.